

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yang, <i>et al.</i>	Attorney Docket:	TSM03-0929
Filed:	Herewith	Examiner:	TBD
Serial No.:	TBD	Art Unit:	TBD
For:	Methods and Structures for Planar and Multiple-Gate Transistors Formed on SOI		

Mail Stop: Patent Application
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P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

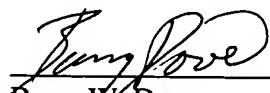
The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A & B that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed concurrently with the patent application.

Pursuant to 37 CFR 1.98(a)(2)(i), as amended, copies of U.S. Patents cited are not being submitted. However, Applicant has included copies of any non-patent literature.

Respectfully submitted,

April 13, 2004
Date



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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	TBD
				Filing Date	Herewith
				First Named Inventor	Yang, <i>et al.</i>
				Art Unit	TBD
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0929
Sheet	1	of	1		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US-6,222,234 B1	04-24-2001	Imai	
		US-6,413,802 B1	07-02-2002	Hu et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		CHAU, R., <i>et al.</i> , "A 50nm Depleted-Substrate CMOS Transistor (DST)," IEDM (2001) pp. 621-624.	
		SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. RES. & DEV., Vol. 46, No. 2/3 (March/May 2002) pp. 121-131.	

Examiner Signature	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.